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An Approach Towards Batch Fabricated Ferrite Memory Planes

Abstract: This paper describes a technique for the batch fabrication of ferrite memory arrays in which wire, previously coated with a thermoplastic, is formed into two orthogonally disposed sets of parallel wires. These grids are oriented between opposing molds having matched grooves filled with a fluid mixture of ferrite powder and thermosetting resin, in such a manner that one set of parallel wires coincides with the groove axes. After suitable curing this structure is released and heat treated to pyrolyze the organic materials and sinter the ferrite.

A yield study on 108 memory arrays produced in this manner resulted in a yield of 72.2% on pulse testing under simulated operating conditions and an over-all process yield of 36.1%. The paper concludes with a tabulation of electrical characteristics of the arrays and a brief discussion of the applicability of the technology to various modes of operation and its potential for high-speed (250 nsec magnetic cycle time) operation.

Introduction

The advantages of batch fabricated ferrite memory arrays have led many workers to seek suitable fabrication technologies. Some notable consequences of these efforts are, at one laboratory, the ferrite apertured plate memory[1] and the more recent laminated ferrite technique[2] and, at another, the ferrite bead[3] and "waffle iron"[4] memories.

Work by the authors and others at this laboratory has resulted in the ferrite flat film memory[5] and, more recently, the development of a new fabrication technique. It is the purpose of this paper to describe this technique, to demonstrate its potential for producing large, prewired arrays of storage elements, and to indicate its technical feasibility by presenting results from a yield study of a number of 5000-element arrays. Some remarks will be made regarding the feasibility of extending this technique to smaller elements requiring small operating currents. A brief description of a device that has been fabricated by the process is given as a preliminary to the discussion of the process itself. Then the testing procedure and results of the yield study are presented, the array characteristics are described and, last, some possibilities for extending the technology are outlined.

Figure 1a **General configuration of the Flute memory element.**

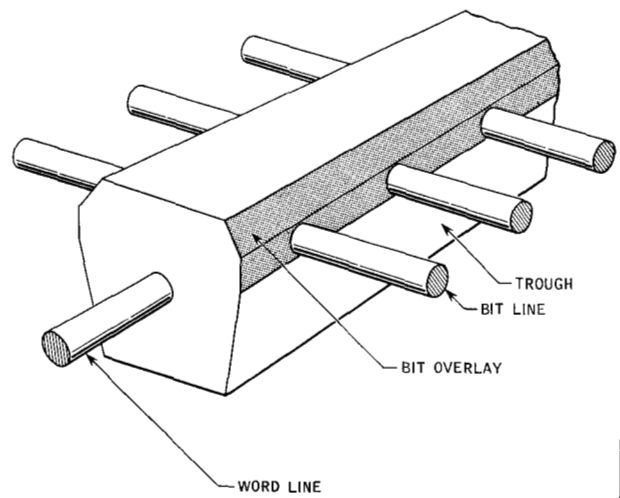
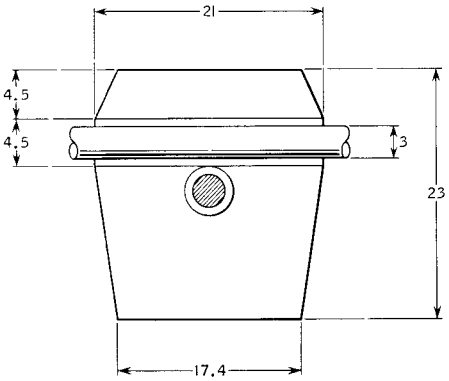


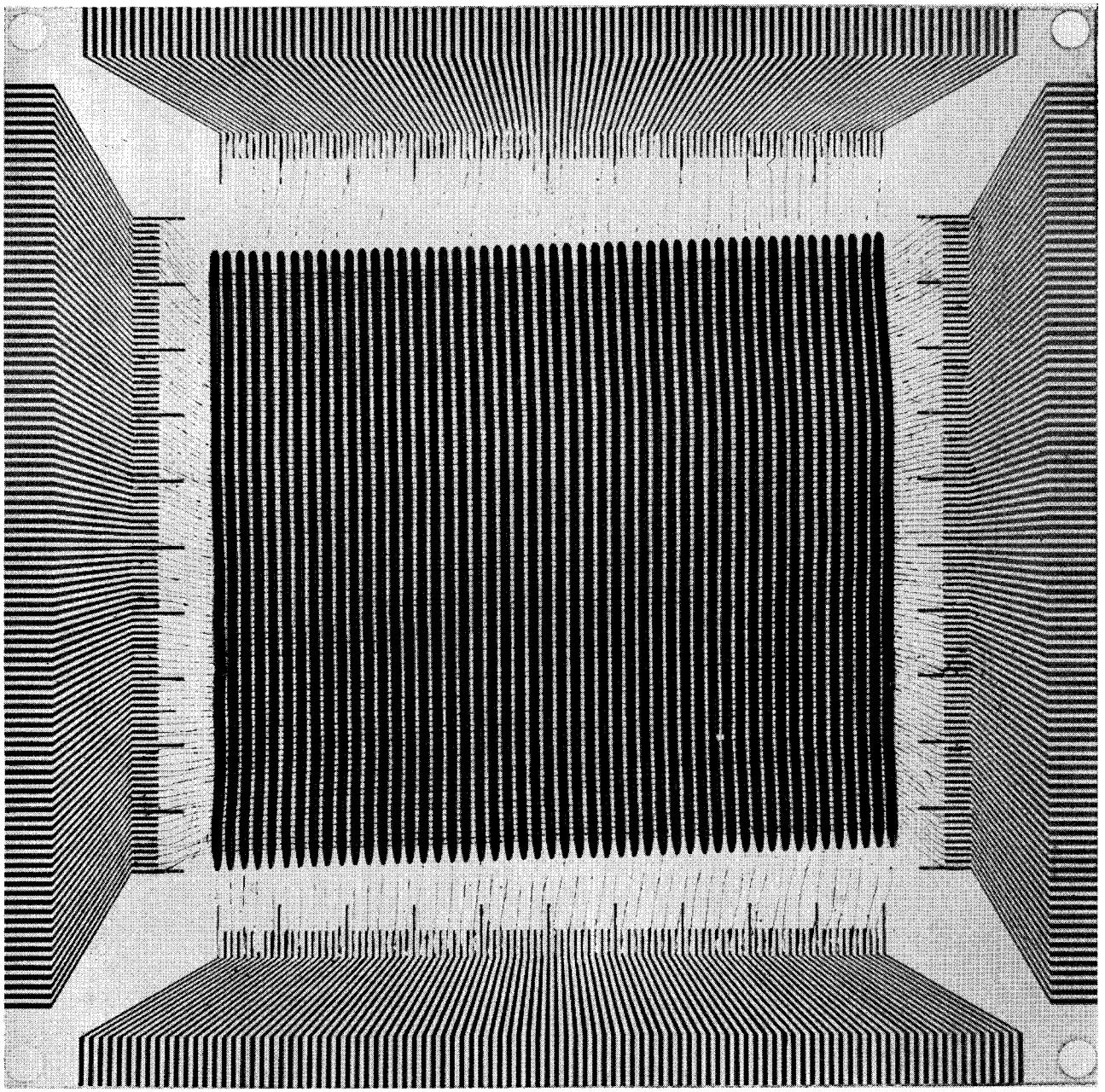
Figure 1b **A cross-sectional view with dimensions given in mils.**



Geometry

The fabricated element considered here is known as *Flute*, in recognition of the fact that its geometry was originally that of a hollow tube having orthogonal circular apertures. It consists of a "tubular" (prismatic) structure surrounding an axial conductor which acts as the word line. The wall of this tube is intersected by a multiplicity of conductors which act as the bit lines. The bit lines are orthogonal to and displaced from the word lines, Fig. 1. A Flute memory plane comprises a number of such tubes that are parallel to one another and are intersected by a continuous set of bit lines. Figure 2 shows such a memory plane containing 50 tubes centered at intervals of 0.070 in. and 100 bit lines centered at intervals of 0.030 in. Both word and bit lines have a diameter of 0.003 in.

Figure 2 **A 50-word × 100-bit Flute memory plane.**



The fabrication process

The design philosophy underlying the choice of geometry of the device and the fabrication process recognizes the degree to which ferrite memory devices are sensitive to adverse chemical and physical effects. Such a process must avoid chemical poisons, afford uniform grain growth, yield a stress-free structure in which critical geometrical tolerances can be maintained and, most important, must be suitable for a high degree of automation.

Flute planes are fabricated by using a matched-die molding process in which a grid of prepared wires is sandwiched and compressed between two dies whose matching grooves are filled with an intimate mixture of a ferrite and a thermosetting resin binder, Fig. 3. This is followed by appropriate curing. Then the plane is released from the molds and sintered, producing a complete and prewired memory plane. Since each of these steps can be automated readily it appears that continuous fabrication and testing would be feasible.

The wire necessary for the process is prepared by coating 0.003 in. 90:10 Ag-Pd alloy wire with a layer of thermoplastic to an over-all diameter of 0.006 in. (This thermoplastic layer melts during the sintering step and thereby creates sufficient space to accommodate ferrite shrinkage.) Next, a very thin (0.0002 to 0.0005 in.) ferrite-filled varnish is placed over the thermoplastic layer to provide electrical insulation between the word and bit lines. Then two sets of parallel wires (word lines and bit lines) are placed in orthogonal relationship to each other and are clamped onto a locating frame. The grid so formed is then positioned between two matching grooved molds, so that each of the 50 word lines coincides with the centerline of the opposing grooves. Some latitude in alignment and wire centering in the word groove is allowable. This results from the fact that the critical dimension is the thickness of the bit overlay, i.e., of the ferrite material lying over the bit line (see Fig. 1 and Appendix 1).

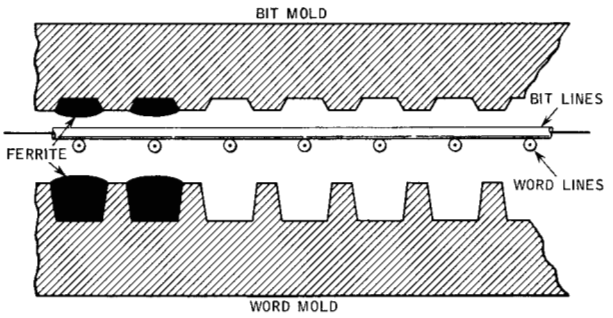
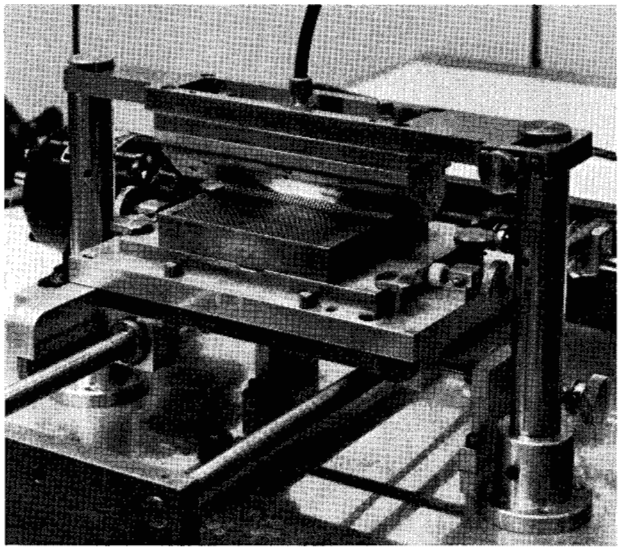
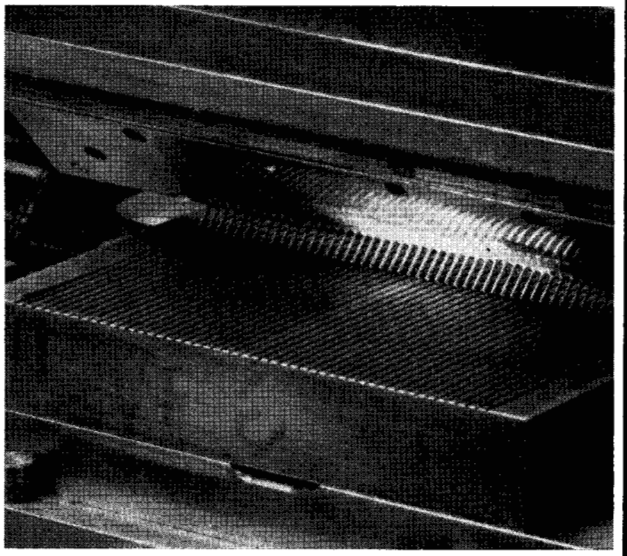


Figure 3 **Cross-sectional view of representative part of the matching molds.** *The small circles represent word lines in position between opposing groves filled with a ferrite/resin mixture.*

The grooves in both halves of the mold are filled with a fluid mixture of ferrite and thermosetting resin (e.g. epoxy resin) by passing them beneath a multiple-needle extrusion device, Fig. 4, which fills the 50 grooves simultaneously. The molds and wire frame are then combined on a locating jig to align the wire frame and both molds properly, Fig. 5. When the molds are compressed the fluid ferrite/resin mixture coalesces, producing a continuous ferrite tube surrounding the word line. The entire assembly is

Figure 4 **(Left) the complete multiple-needle extrusion device for filling mold grooves semiautomatically; (right) the needles and grooved mold shown in greater detail.**





subjected to a cure cycle, in which the ferrite/resin mixture gains sufficient mechanical strength to be safely removed from the molds. The green Flute array then undergoes a heating cycle which accomplishes the following: first, the thermoplastic wire coating melts and drains from the tubes; next, as the temperature is increased, the organic binder undergoes oxidative pyrolysis, leaving a binder-free ferrite structure; finally, sintering at the ultimate cycle temperature (920-940°C) produces a completed, prewired array.

Testing and yield

Process variables such as are introduced by modifications to materials, geometry, dimensions, and sintering have been investigated using a semi-automated fabrication line. After their influence was understood and subject to control, it was possible to undertake studies of yields. A number of arrays were produced for this purpose using 12 separate mold sets and 3 separate batches of ferrite powder and batch firings. Testing was performed in several sequential stages so that the bulk of defective arrays could be eliminated early in the process. In brief, these stages consisted of a physical examination of the molded structure before firing, a second physical examination immediately after sintering, a measurement of coercive force, tests of wire continuity and insulation, and, finally, an electrical-pulse operational test. These tests are discussed at greater length below.

Directly after release from the molds, the arrays are inspected for mechanical defects, both visually and with an x-ray shadowgraph which allows detection of displaced word lines and internal defects in the ferrite structure.

After several arrays are sintered simultaneously (in an electric kiln constructed to have a uniform (±2°C) temperature profile in a 6 × 6 × 6 in. volume) they are examined visually for mechanical defects. A measurement is made of the coercive force H_c, which must be held within narrow limits to pass the yield test. Next, all arrays are checked for electrical continuity and the adequacy of the insulation between bit and word lines. Arrays passing these preliminary tests are then attached to printed circuit terminal boards, which are required to adapt the arrays for insertion into automatic pulse testing equipment.

A prime criterion for evaluating the fabrication technology was the number of acceptable bit junctions produced per memory plane; this was determined by a testing procedure which simulated the most adverse read-write conditions that can exist in a real, word-organized memory system. The procedure employed a pulse pattern, shown in Fig. 6, which includes the effects of very severe read-write conditions and variations (±10%) of all current amplitudes. The first precycle sequence establishes a strong 0 state prior to writing, disturbing, and reading a weak 1 signal. The second precycling sequence establishes a strong 1 state prior to writing, disturbing, and reading a weak 0 signal.

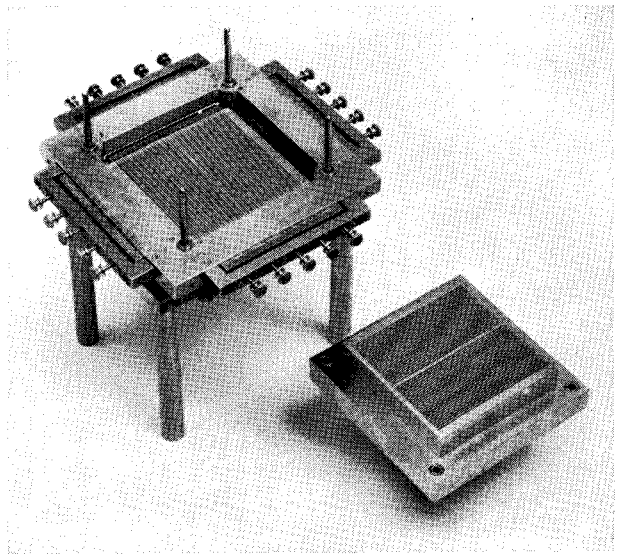


Figure 5 **A stage in the molding process.** *Grooves in both molds have been filled with ferrite/resin mixture; one mold and the wire grid are in position on the locating jig.*

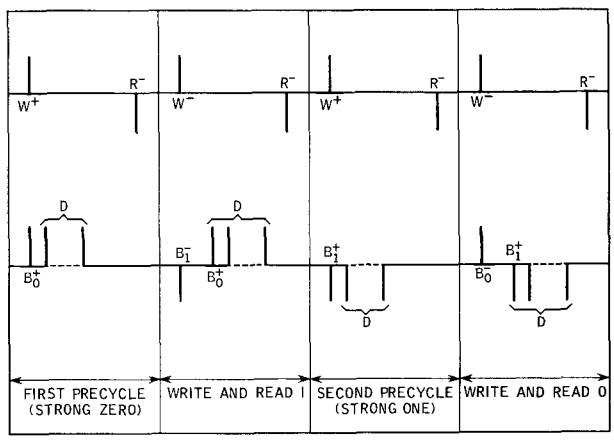


Figure 6 **Pattern for pulse testing fabricated elements.** *In this figure W denotes a word pulse; R, a read pulse; and D, a disturb pulse. B_0 and B_1 denote* **0** *and* **1** *bit pulses, respectively. Nominal values of current were as follows: I_W = 330 mA; I_R = 600 mA; I_B for* **1** = 96 mA; *and I_B for* **0** = 73 mA. *Where they appear, plus or minus signs indicate ± 10-percent deviations from nominal current values.*

The pulse test applies pulses to and records outputs from every bit location in the array, with contacts being made to the array by means of an automatic stepping

Table 1 **Yields after five stages of testing.**

Test stage	*Number tested*	*Number accepted*	*Percent accepted*
Visual and x-ray examination of green, molded arrays	108	72	66.6%
Visual examination after sintering	72	70	97.2
Measurement of coercive force H_c	70	59	84.2
Continuity and insulation testing	59	54	91.5
Electrical pulse testing	54	39	72.2
Cumulative results	108	39	36.1

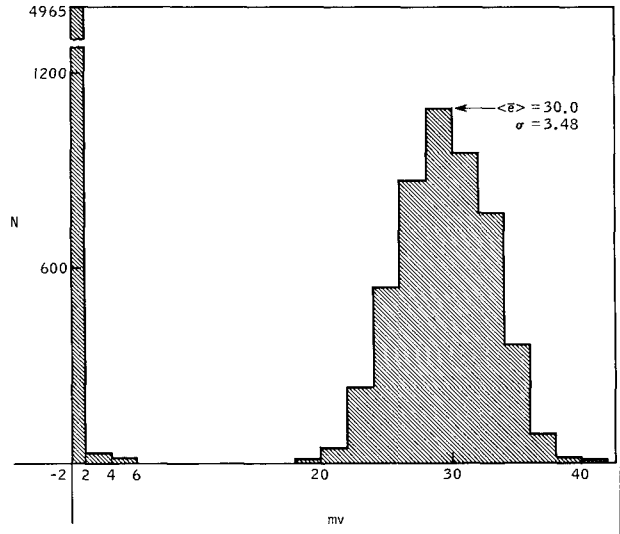


Figure 7 **A histogram showing the distribution of output voltages and the degree of discrimination between 1 and 0 signals.**

mechanism. Outputs are detected using a peak-level detector, gated at read time to eliminate bit noise during write time. These outputs are recorded as a visual display on an electric typewriter, and as a punched paper tape which is used for computer data reduction.

The IBM 7094 was used to analyze the data from each array and to compare it with various selection criteria. Those used for the yield study were that the 1 signal must be equal to or greater than 18 mV and the 0 signal must be equal to or less than 6 mV. Additionally, all of the unacceptable bit locations must be located on word or bit lines whose total number does not exceed 10% of those in the array; that is, 45 of 50 word conductors and 90 of 100 bit conductors could be chosen to define an array of 4050 bits, each having a 1 output greater than 18 mV and a 0 output less than 6 mV. This criterion for line selection is a consequence of the wiring scheme discussed in Appendix 2.

A histogram, Fig. 7, was plotted for each array to show the distribution of the outputs. A mean and a standard deviation were also calculated. The histogram emphasizes the high degree of discrimination obtained between the 1 and 0 signals. The histogram for the 0 signal does not have the shape that might be expected because the peak level detector had a threshold of 2 mV, and treated all outputs below this value as being 2 mV.

Table 1 summarizes the results of the yield study by listing the number and percent of arrays accepted after each process step. The yield for the over-all process was 36.1%, and the yield after pulse testing was 72.2%.

Characteristics of the arrays

A series of experiments were performed to determine the electrical characteristics of arrays examined in the yield study. These are summarized in Table 2.

Table 2

Read current	−600 mA
Write current	+330 mA
Bit current for 1	+ 96 mA
Bit current for 0	− 73 mA
Output signal for 1	30 mV
Output signal for 0	− 10 mV
Characteristic impedance[a]	190 Ω
Back voltage[b]	200 mV/bit
Word-to-bit capacitance[c]	1 pF
Wire resistance	4.2 Ω/ft
Insulation breakdown	>200 V/mil

[a] Word line impedance measured using both a pulse method described by P. Emile (Ref. 6) and a steady state impedance measurement.
[b] Back voltage at read time for a 600-mA read current with a 100-nsec risetime.
[c] Capacitance measured by applying a current to the word line and measuring the time constant of the circuit formed by connecting the bit line to ground through a known resistance.

Some implications of the technology

- *Modes of operation*

The electrical mode of operation used in the Flute yield study employs bipolar word currents (opposite-polarity read and write currents on the word line), and bipolar bit currents (opposite-polarity bit currents for writing a 1 and a 0). The Flute memory has the capacity of operating using a unipolar word current (with the same polarity and amplitude for reading and writing) and a unipolar bit current (with writing performed by either the presence or absence of the bit current at write time). This last mode

of operation offers an important advantage in that it reduces the complexity of the drive circuitry; however, for the same amplitude word current (600 mA) the output signals are smaller (20 mV for **1**, 3 mV for **0**) than those in Table 2. In addition to its ability to use either bipolar or unipolar currents, the Flute also has a capability for high speed nondestructive read operation.[7]

- *Packing density and current requirements*

Planes containing bits having 33 word lines per in. and 50 bit lines per in., Fig. 8, have been made by reducing the spacing of the elements previously described. Experimental elements much like Flute have been made with an outer diameter of 0.005 in. These have been operated in the bipolar-word, bipolar-bit mode with currents less than 100 mA and have output signals greater than 5 mV. It appears reasonable to expect that word and bit line spacings of 100 per in. are feasible with this 0.005 in. element.

- *High speed operation*

High speed operation (250 nsec magnetic cycle time) of the Flute is possible. Elements similar to those used in the yield study have been operated in a read-write cycle at a 4 Mc repetition frequency. The currents used and the outputs obtained are shown in Table 3 (overleaf).

Conclusions

A new process for batch fabricating ferrite elements has been developed. The results of a yield study on more than 100 arrays containing 5000 bits have been presented to

Figure 8 **A 98-word × 150-bit Flute plane.**

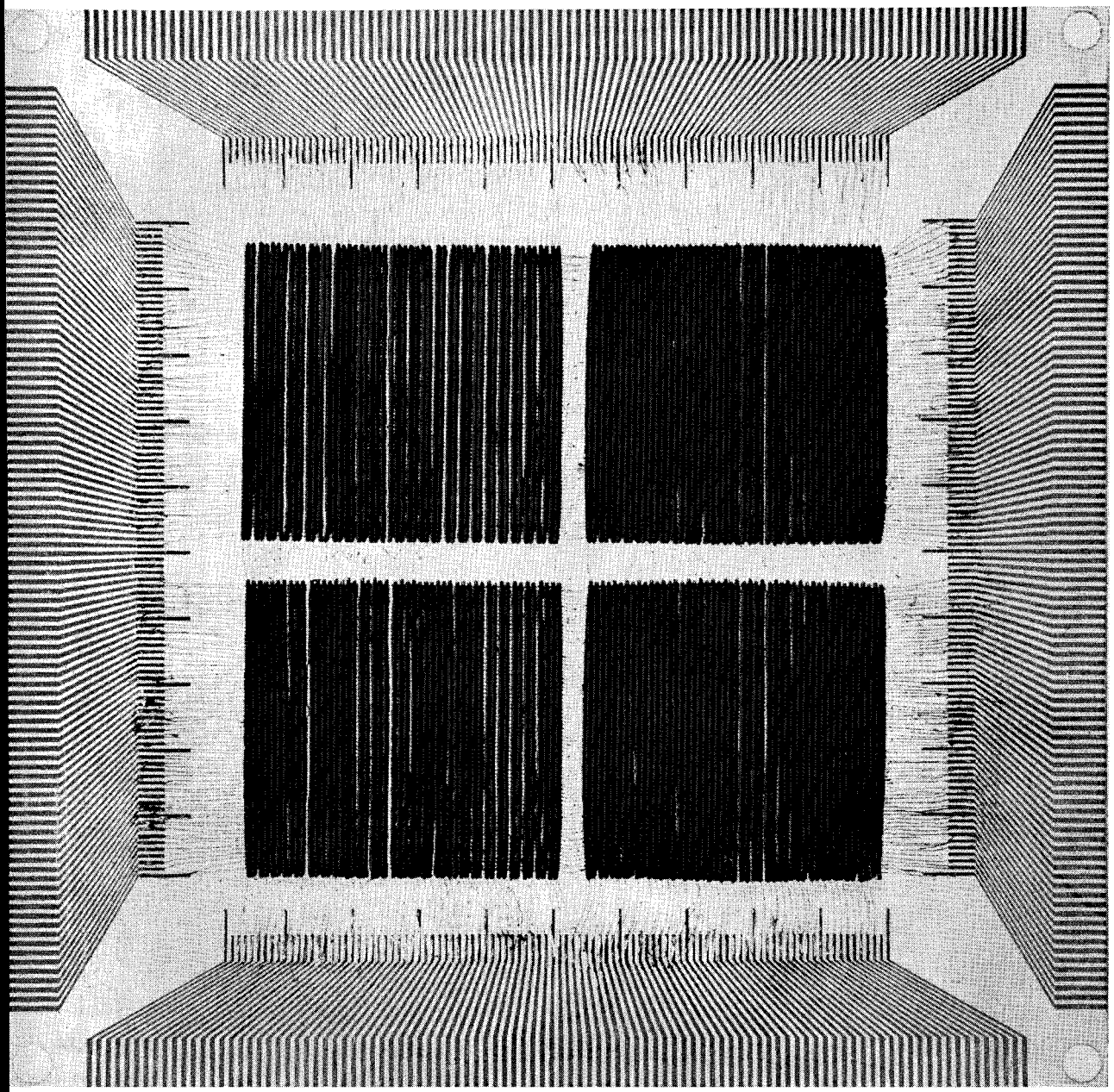


Table 3 **Operating currents and observed outputs, operation at a 4 Mc repetition frequency.**

Read current	−800 mA for 150 nsec, 30 nsec rise time
Write current	600 mA for 50 nsec
Bit current for 0	25 mA for 70 nsec
Bit current for 1	80 mA for 70 nsec
Output for disturbed 1	60 mV
Output for undisturbed 0	−38 mV
Output for disturbed 0	0 mV.

demonstrate its technical feasibility. Smaller elements have been successfully operated; in size and current requirements these elements are compatible with large prewired high density (10^4 bits/in^2) memory planes operable with small currents (100 mA). In addition, memory planes suitable for high speed operation (250 nsec magnetic cycle time) have been developed.

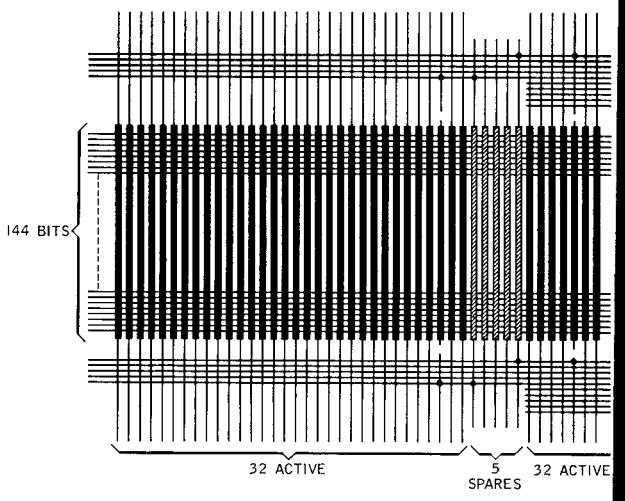


Figure A-1 **Scheme for modifying arrays to accommodate the presence of non-operable bit locations.**

Appendix 1

A series of experiments was performed to determine which of the geometric parameters require accurate control to ensure uniform outputs from element to element. The 1 and 0 outputs were measured for every junction in each word tube of a Flute array in which the material overlying the bit lines (the "bit overlay") had various thicknesses. After pulse measurements were made, the word tubes were removed from the array and carefully sectioned. A photomicrograph was taken at each bit junction and thicknesses of the bit overlay and tube wall were measured. It was found that the measured outputs were directly proportional to the minimum thickness of the bit overlay for all junctions where the bit overlay thickness was less than that of the tube wall. So to obtain uniform outputs it is necessary only to control the bit overlay thickness so that it is less than the tube wall thickness.

Appendix 2

A problem inherent in any large batch fabricated memory technology is the presence of non-operable bits. This "bad bit" problem can be alleviated by using a new scheme for automatic testing and wiring.[8] Figure A-1 shows the array divided into sets of n_1 adjacent tubes, which will be called "active" tubes. Between these sets are n_2 "spare" tubes. Active word-tube conductors are attached to the external frame while spare tube conductors lie over the printed "jumper" lines. These jumper lines are electrically insulated from the word lines. In applying this scheme, the first tube of the first active set is fully tested. If it is accepted, testing proceeds to the second tube, etc. When a tube is rejected (for example, Tube 30 in Fig. A-1, where $n_1 = 32$ and $n_2 = 5$) its conductor is first welded to a jumper line and is then broken between the weld and the tube to isolate the defective tube. The tester now proceeds to the first spare tube and tests it fully. If it is acceptable, its conductors are welded to the same jumper lines. If the first spare tube is rejected, testing proceeds to the second, etc. Testing now returns to Tube 31, and proceeds through the array, internally substituting spare tubes for defective active tubes. The same wiring scheme can similarly be applied in the bit direction. Thus, by fabricating arrays of appropriate oversize, planes having 100% active storage can be produced.

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